

FIG. 1a  
(Prior Art)

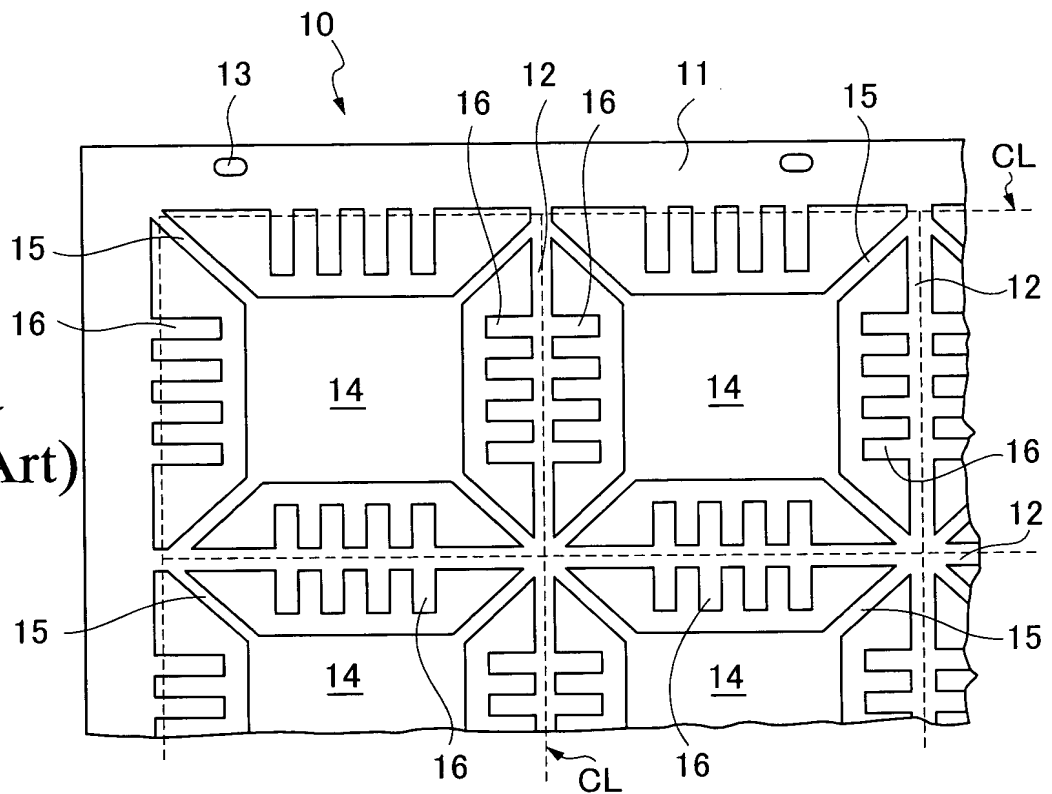


FIG. 1b  
(Prior Art)

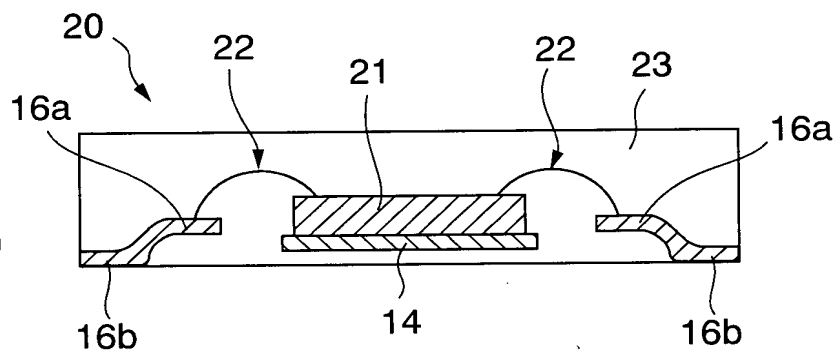


FIG. 1c  
(Prior Art)

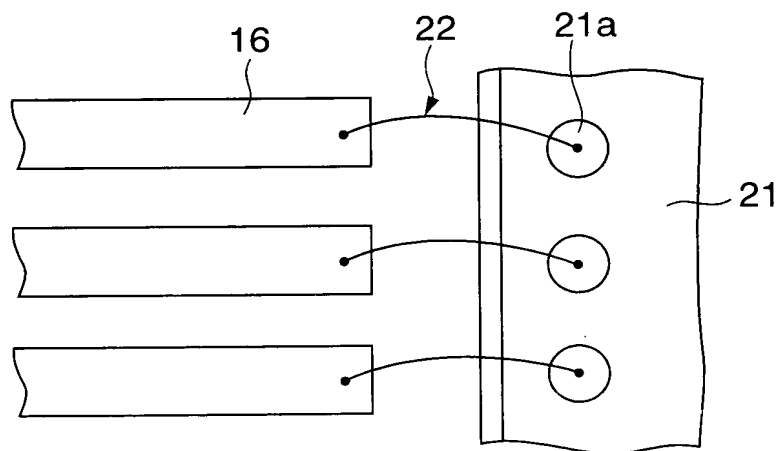


FIG. 2a

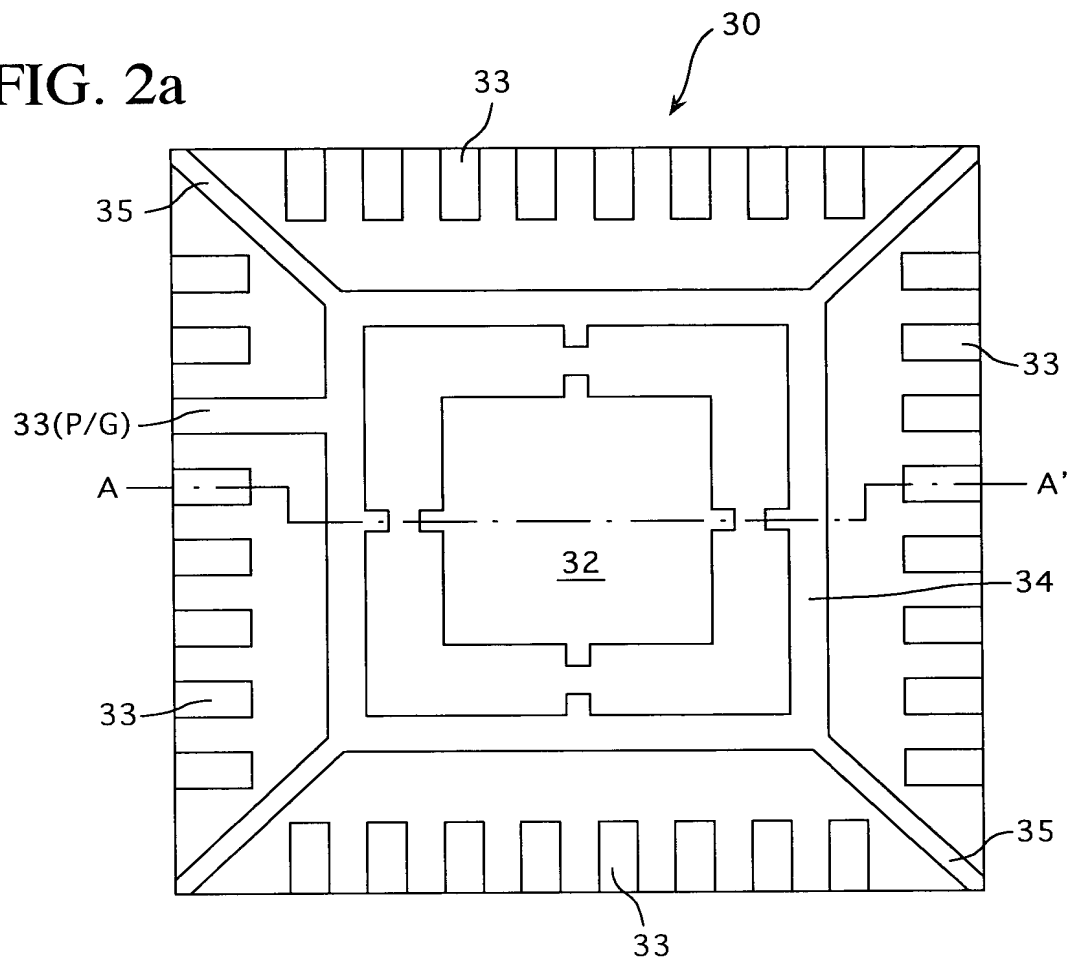


FIG. 2b

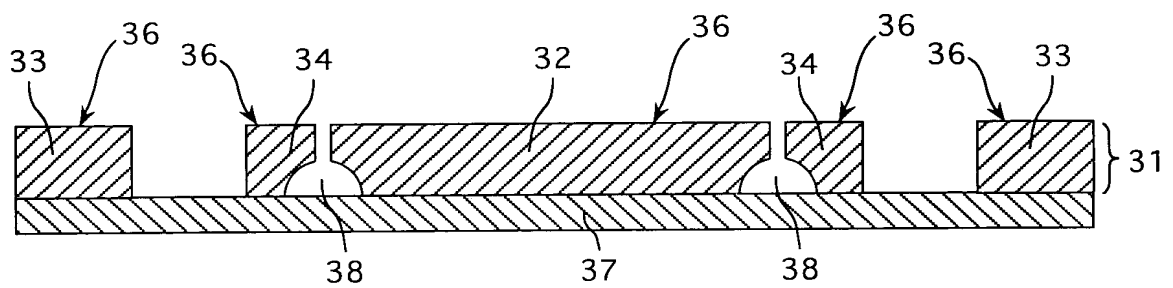


FIG. 3

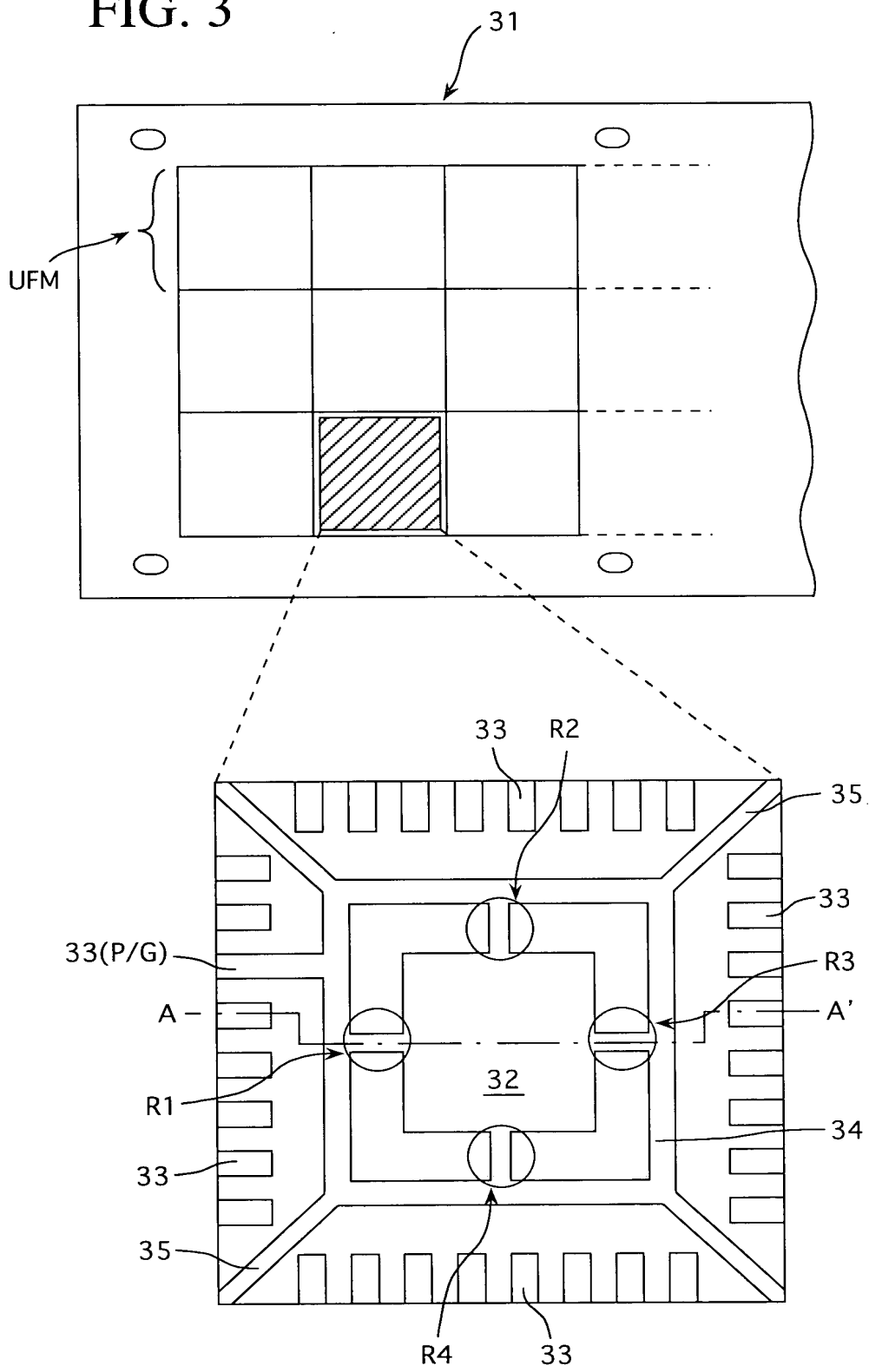


FIG. 4a

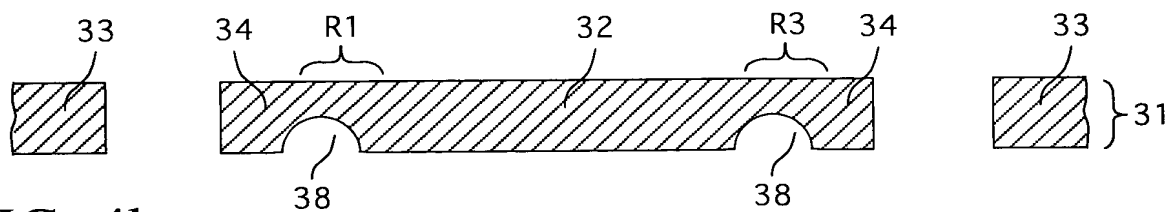


FIG. 4b

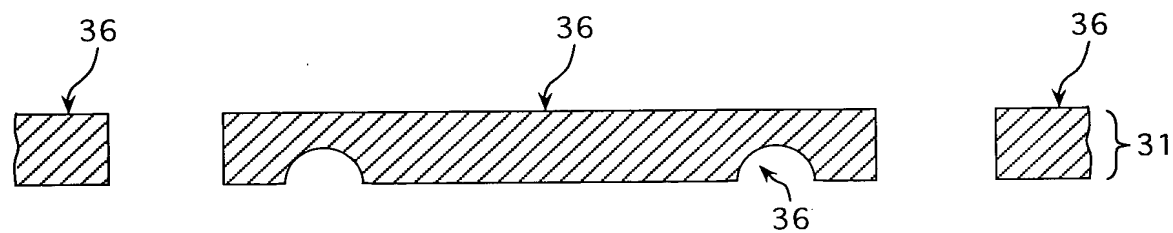


FIG. 4c

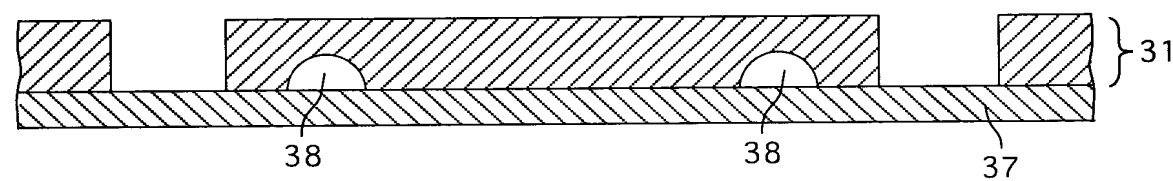


FIG. 4d

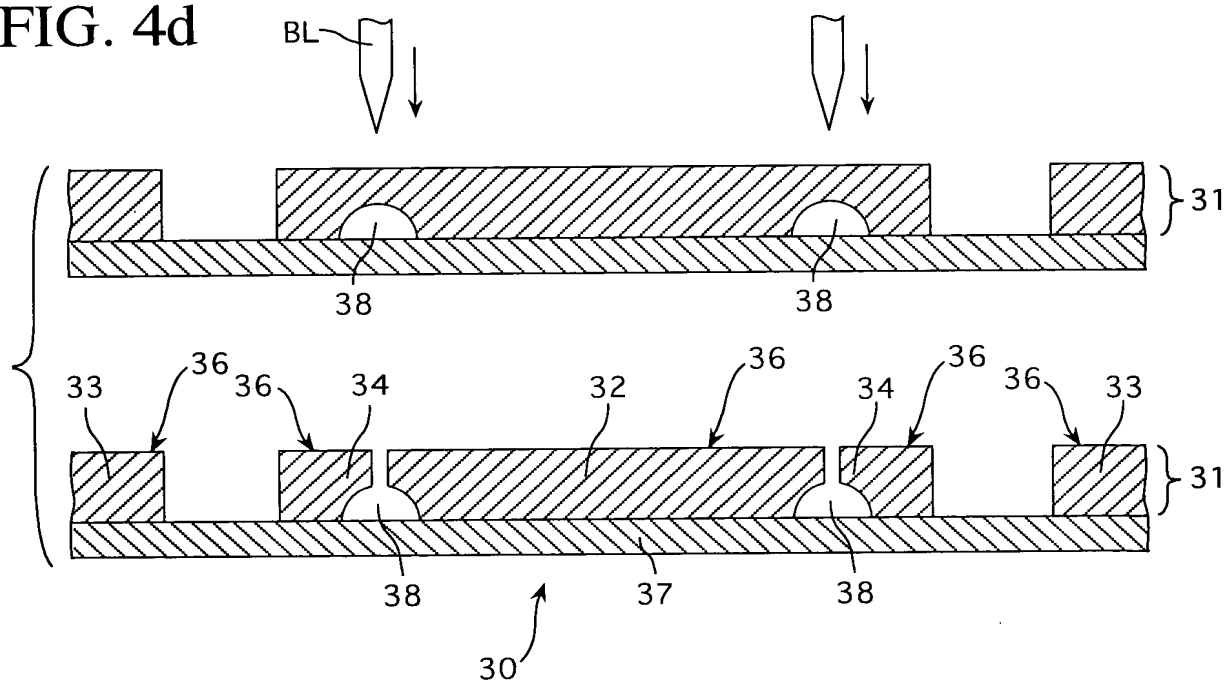


FIG. 5a

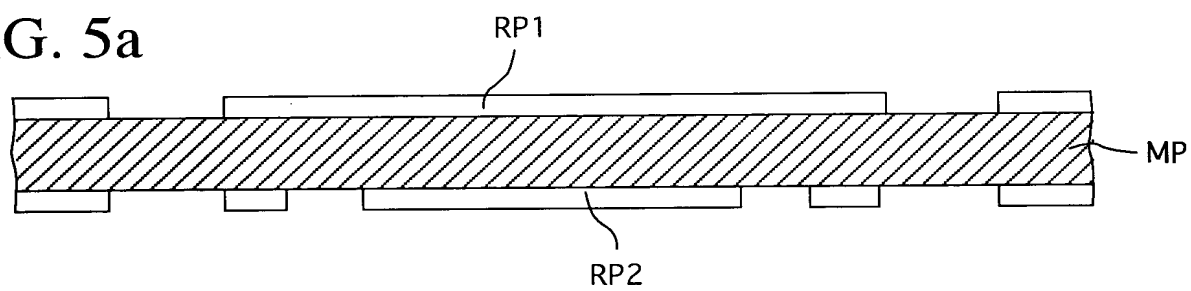


FIG. 5b

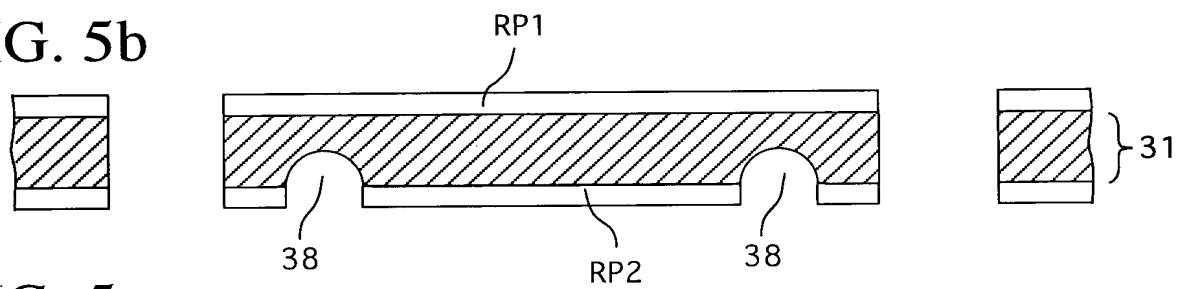


FIG. 5c

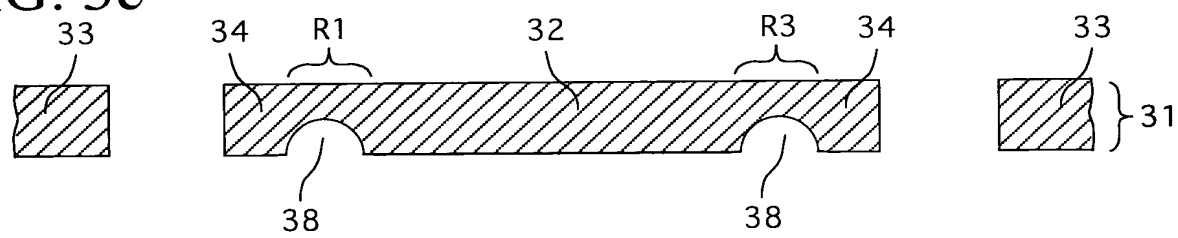


FIG. 6a

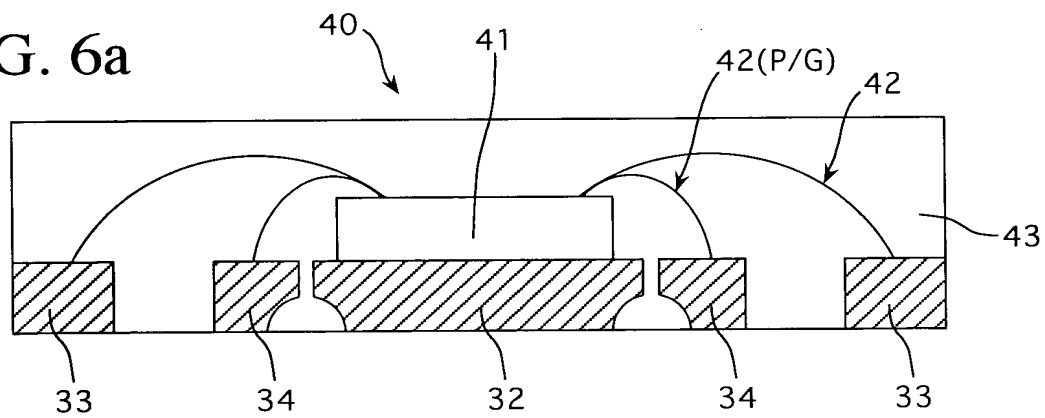


FIG. 6b

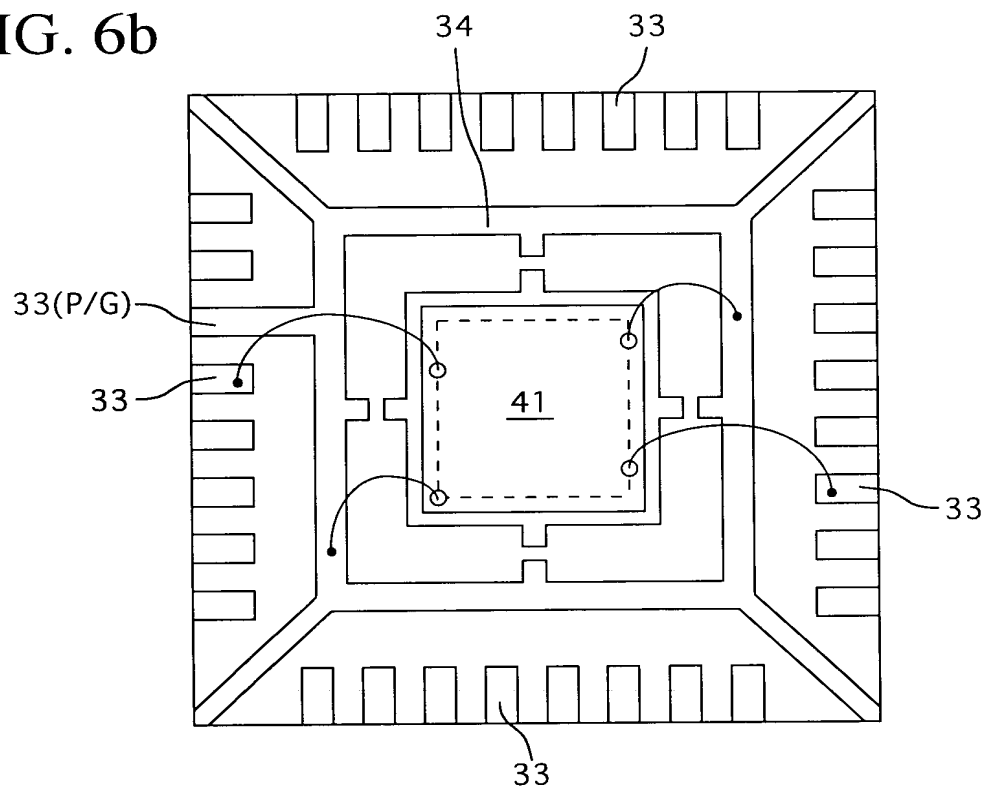


FIG. 7a

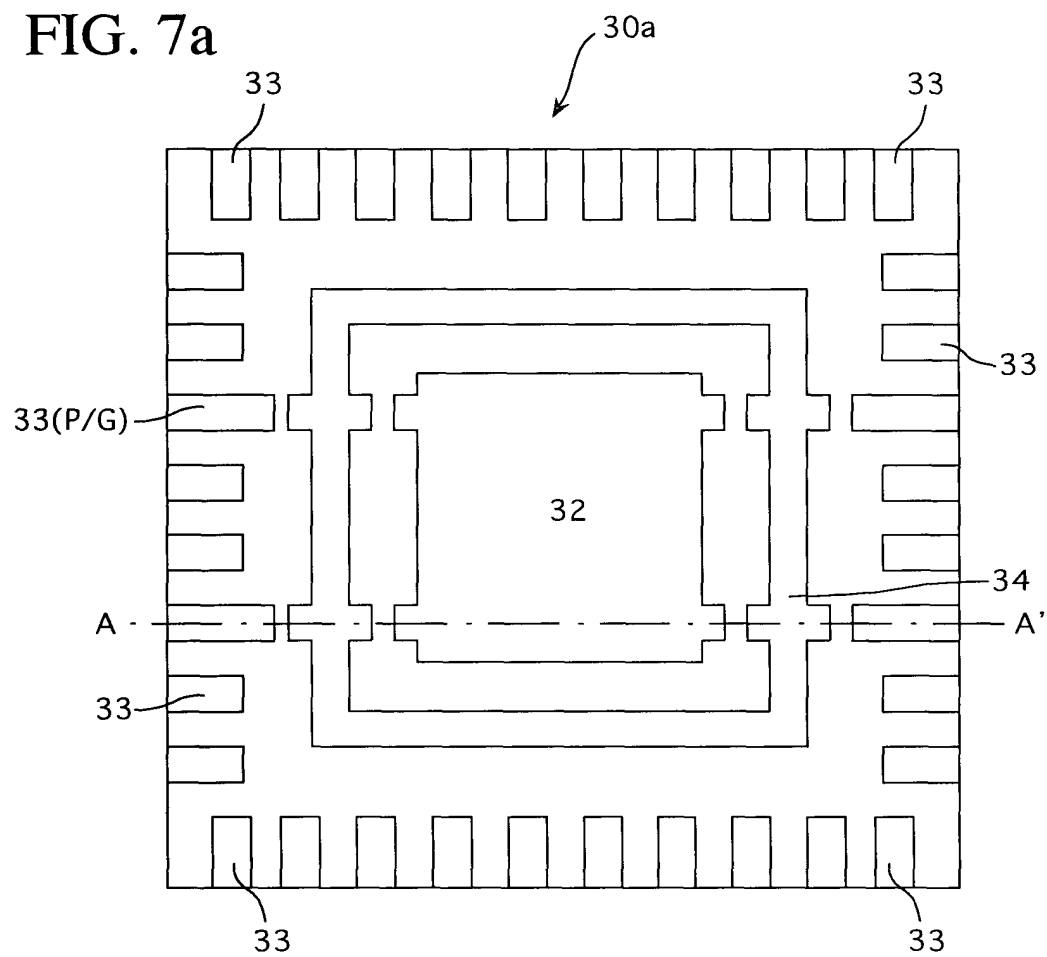


FIG. 7b

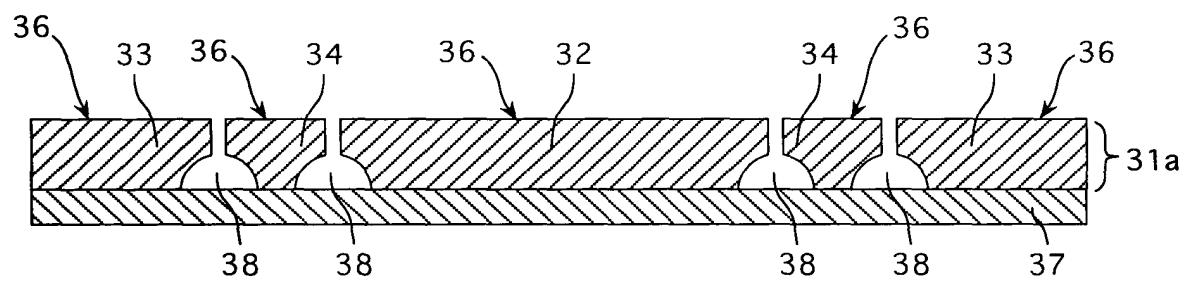


FIG. 8

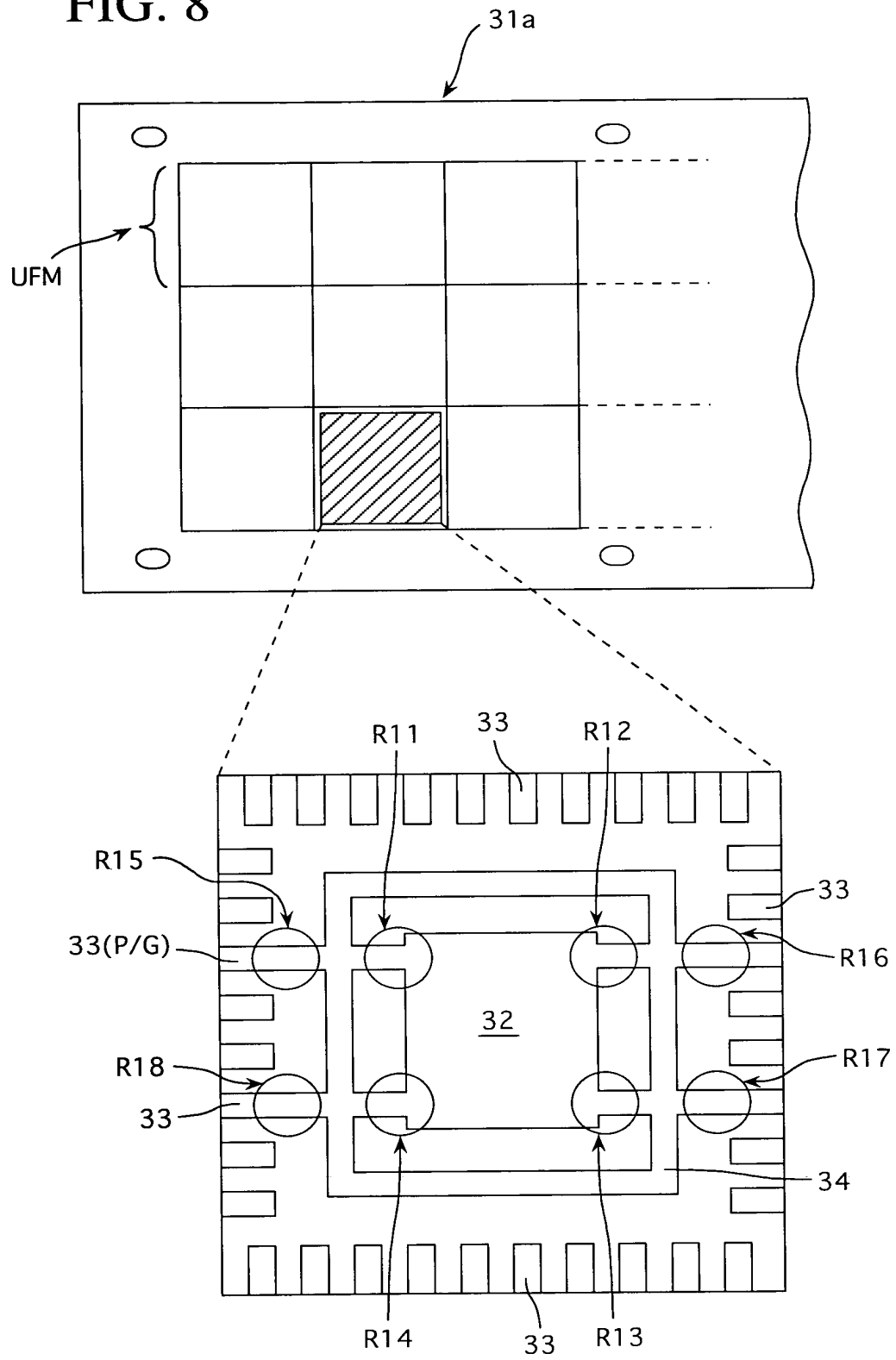




FIG. 9a

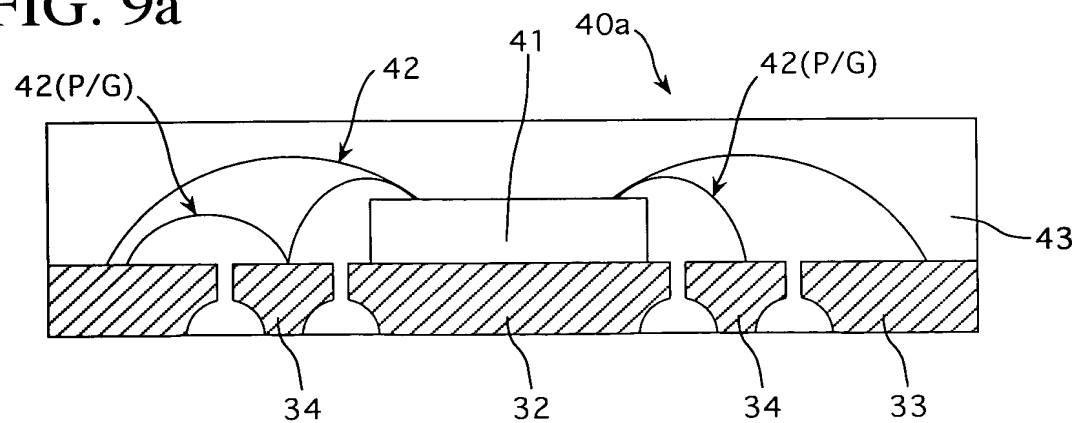
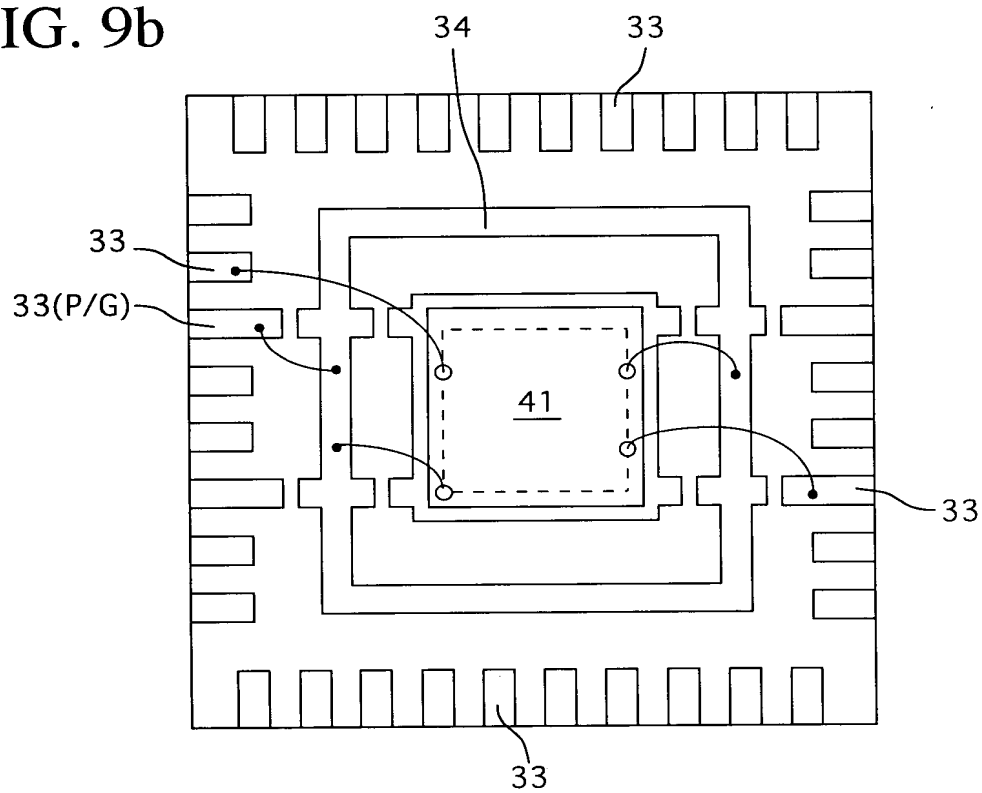


FIG. 9b



**FIG. 10a**

FIG. 10a is a top-down schematic diagram of a square device 30b. The device features a central square region 32, a surrounding rectangular frame 34, and a thick outer border 33. The border 33 is composed of a top and bottom row of rectangular blocks, and side rows of blocks labeled 33(P/G). Diagonal lines 35 are shown in the corners. A horizontal dashed line A-A' passes through the center of the device.

FIG. 11

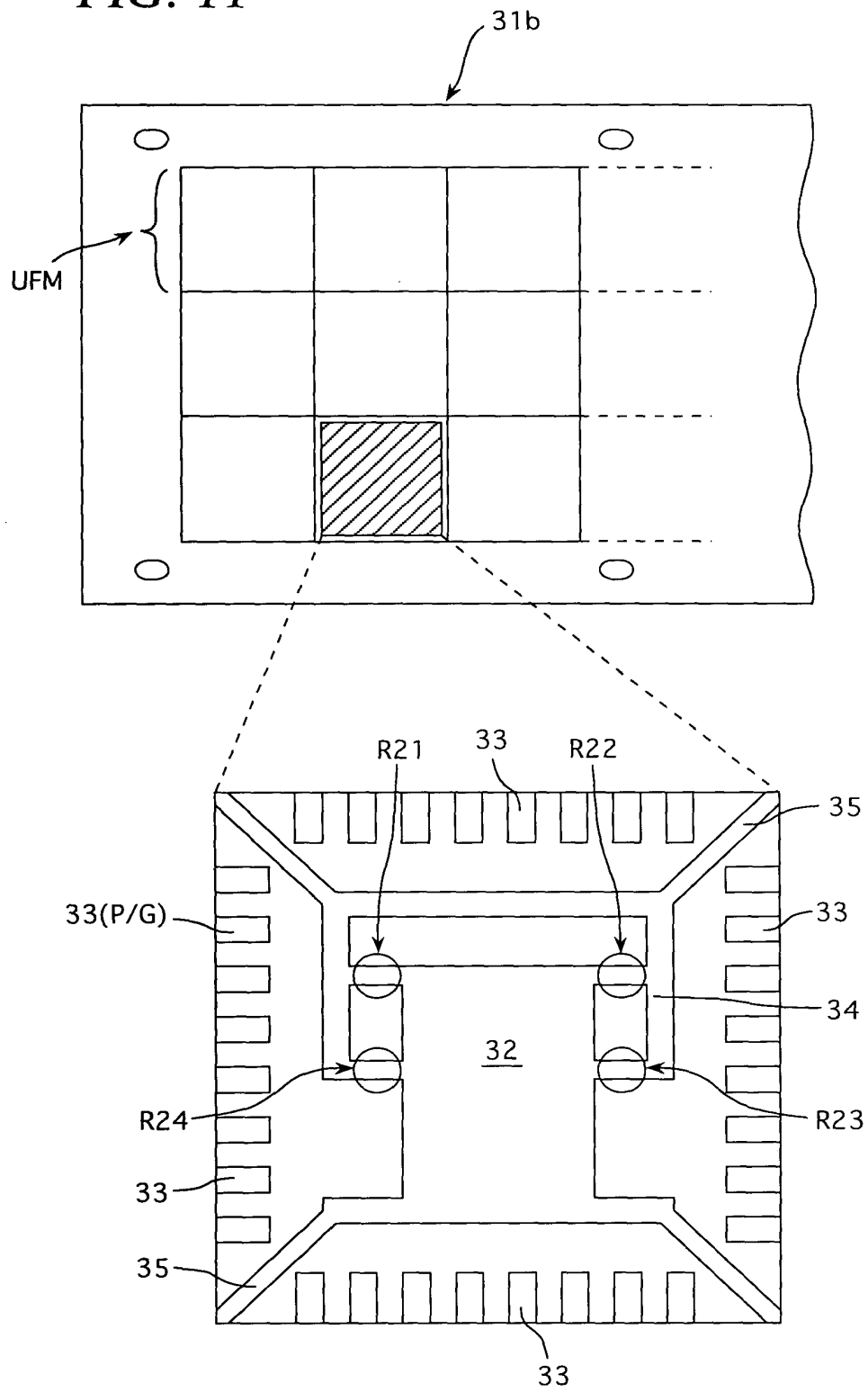


FIG. 12a

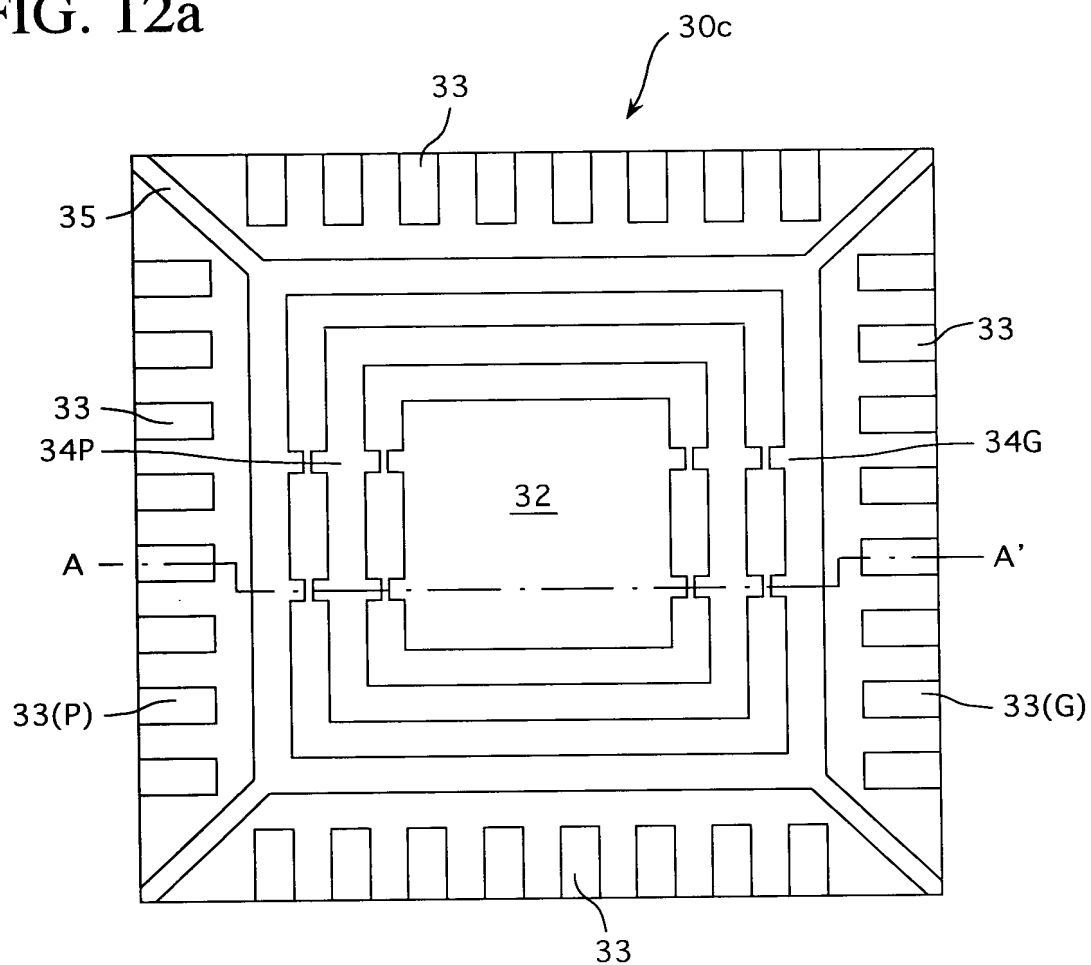


FIG. 12b

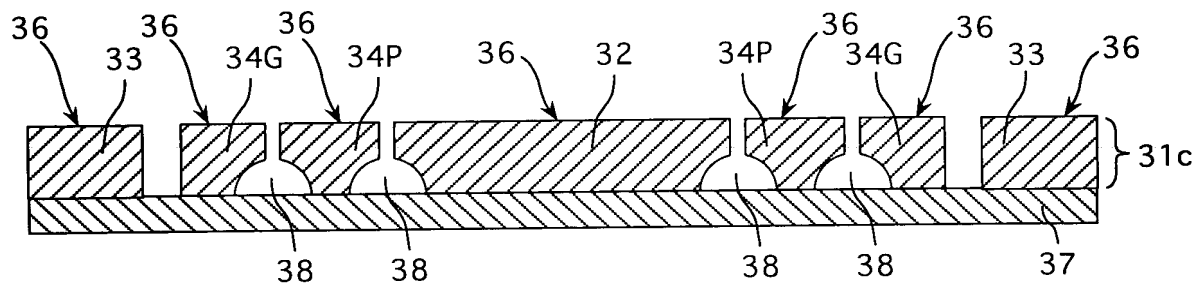


FIG. 13

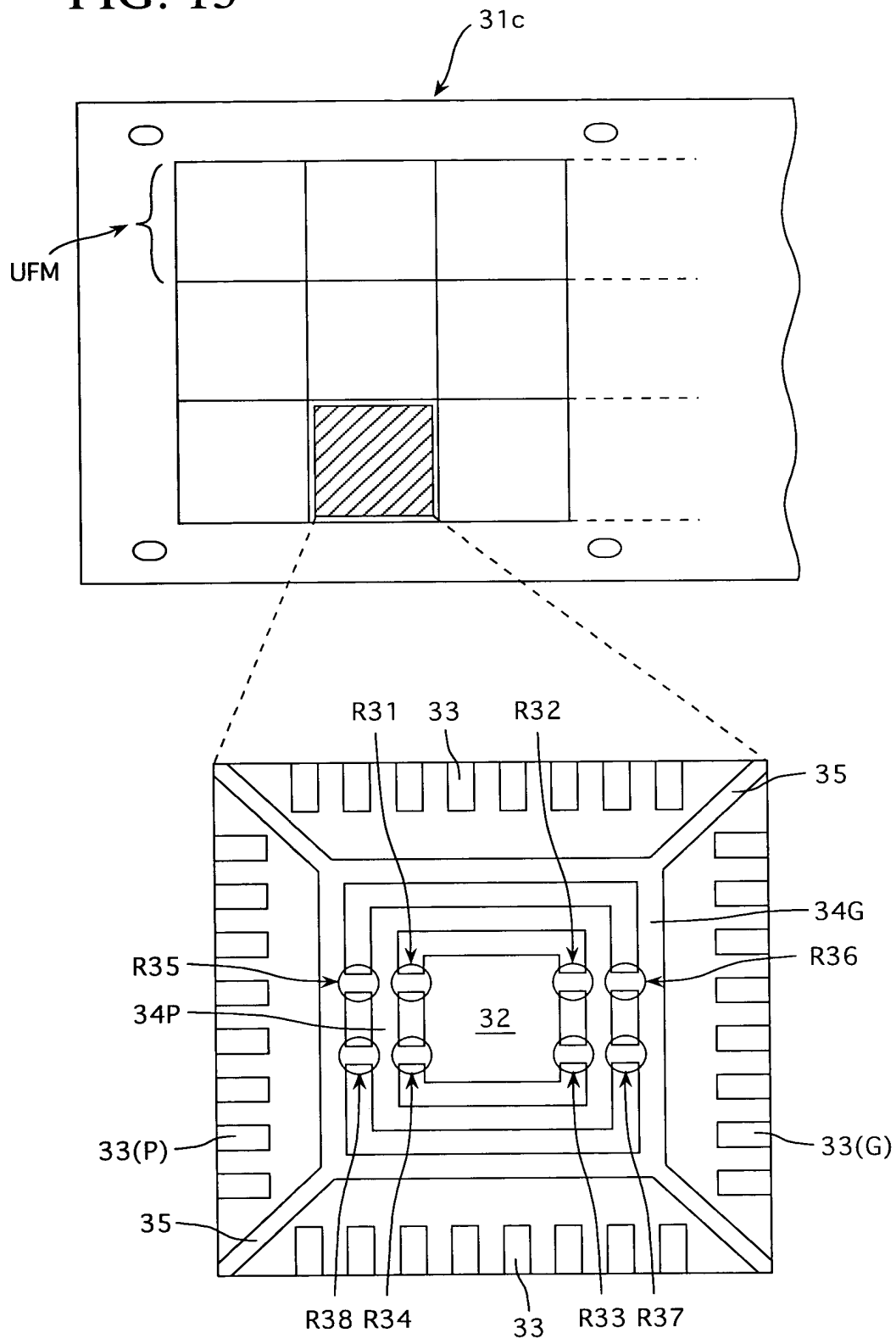


FIG. 14a

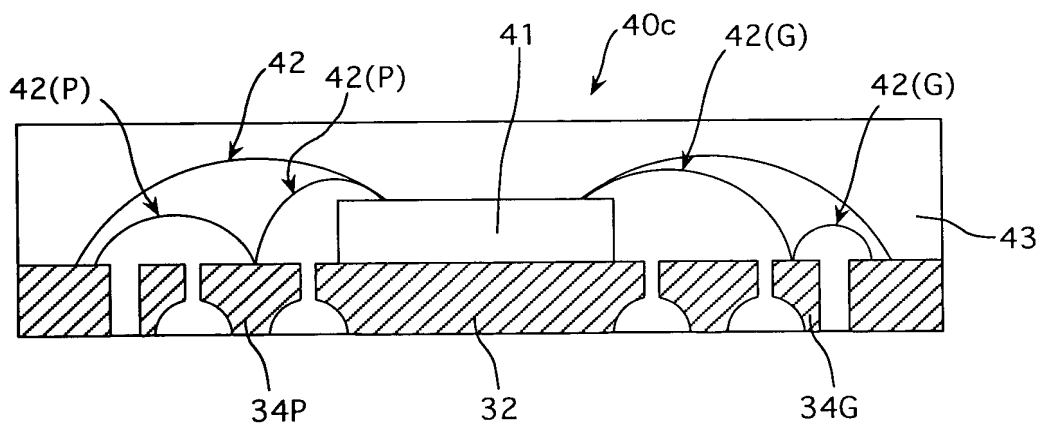


FIG. 14b

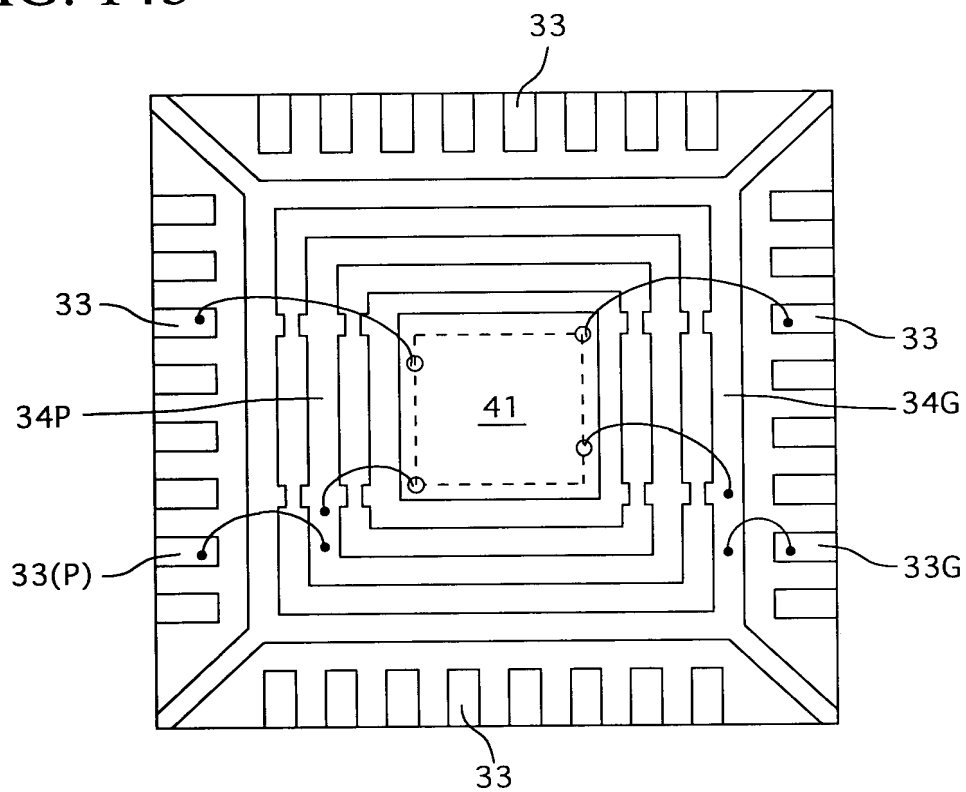


FIG. 15a

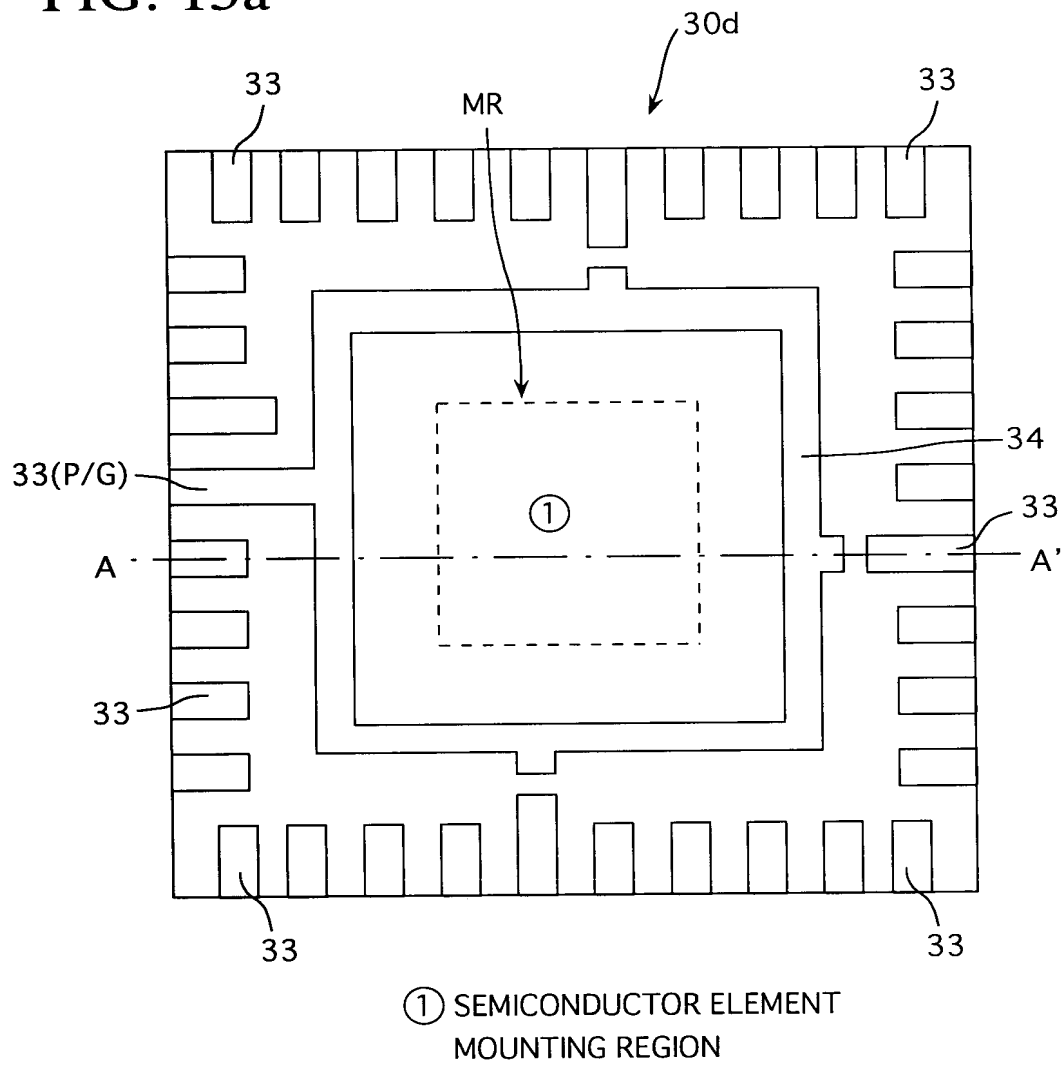


FIG. 15b

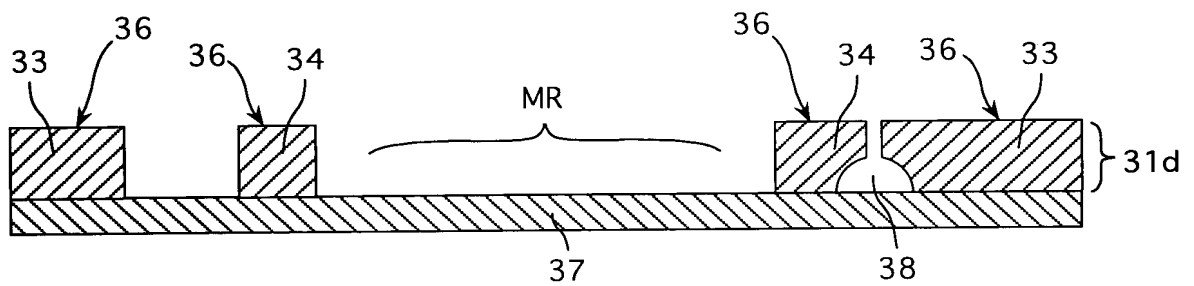
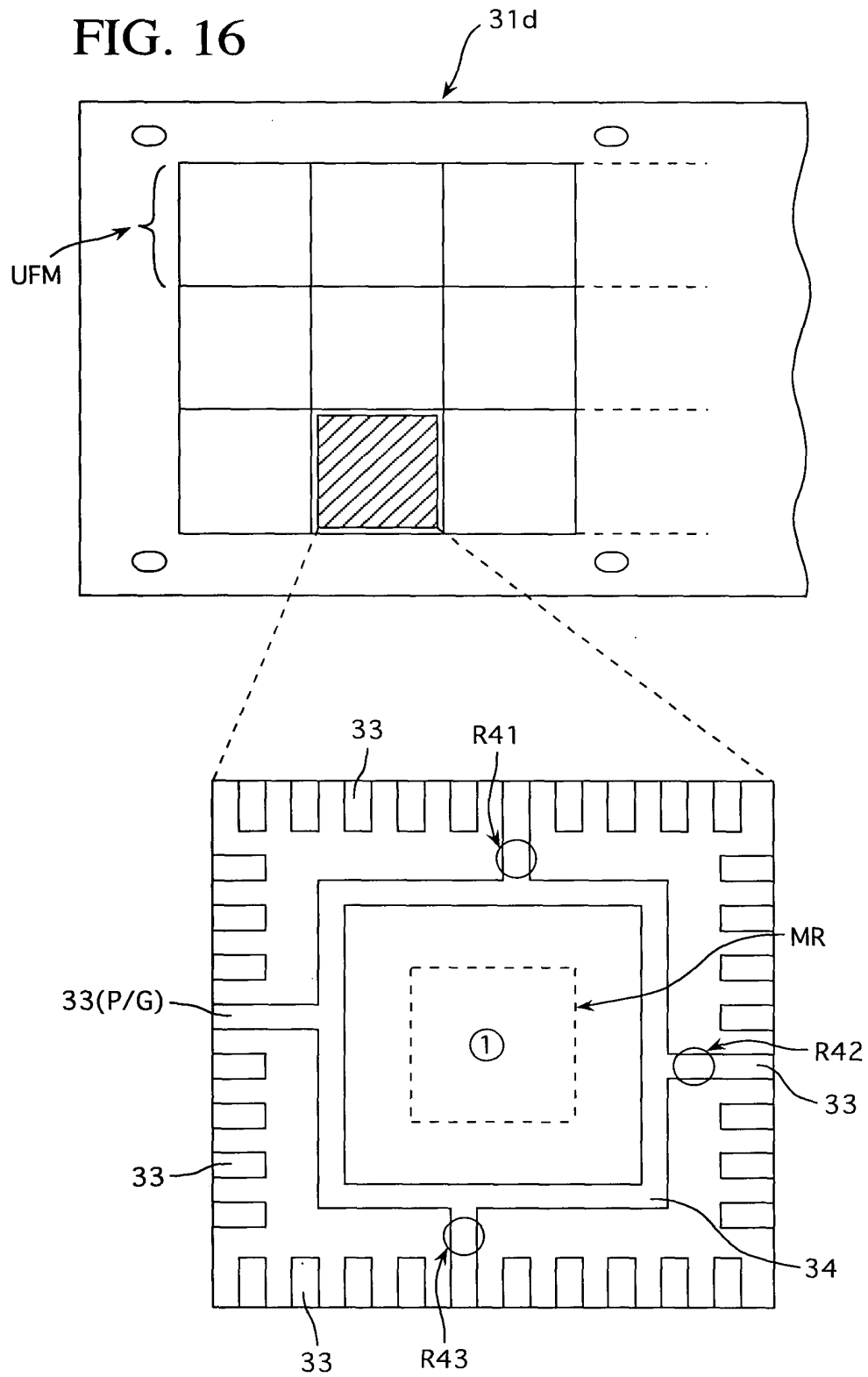


FIG. 16



① SEMICONDUCTOR ELEMENT  
MOUNTING REGION



FIG. 17a

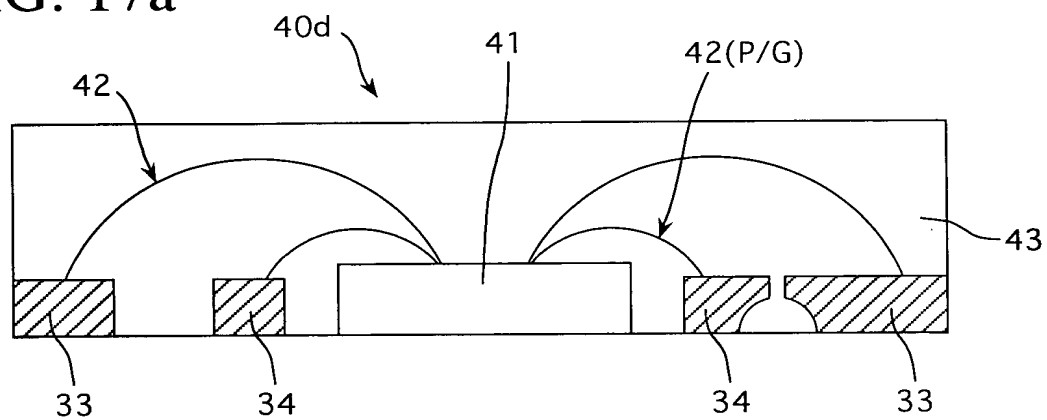


FIG. 17b

